EUROPEAN COOPERATION IN SCIENCE AND TECHNOLOGY

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COST Action no. IC1204 2012 | 2016

TRUDEVICE

Trustworthy Manufacturing and Utilization of Secure Devices

Information and Communication Technologies (ICT)

Participating countries: 19

BE, CH, CZ, FI, FR, DE, GR, IL, IT, NL, NO, PT, SK, SI, SP, SE, MK, TR, UK

Objectives

- **To identify new design and manufacturing flows for the production of secure integrated circuits by creating a strong network between several centers of expertise on hardware security at European level**
- To provide solutions for required but conflicting relationships between Testability and Security.
- To study new mechanisms for devices identification and authentication based on the usage of Physically Unclonable Functions (PUFs) and True Random Number Generators (TRNGs)
- To address issues related to counterfeiting and Hardware Trojan insertion and to propose new methods and algorithms for their identification
- To define new architectures able to detect faults and to resist to fault attacks

Working Groups

- **WG1: Manufacturing test of secure devices**
  - Tools and methodologies to improve test production coverage for secure functions
  - Secure protocols and controllers to protect the access to necessary test infrastructures
  - Extending security for IEEE system-level test standards
- **WG2: Trustworthy manufacturing of secure devices**
  - PUFs for precise identification of secure devices
  - Hardware Trojan detection
- **WG3: Fault attack detection and protection**
  - Using redundancy to detect fault attacks
  - Cross-level optimizations on residual weak spots in the circuit
- **WG4: Reconfigurable devices for secure functions**
  - Mitigation architectures on FPGAs to counteract fault attacks
  - Self-repairable architectures of secure devices
- **WG5: Validation, Evaluation, and Fault Injection and Simulation**
  - Fault-injection campaigns
  - Fault simulators for realistic fault-models
  - Validation and Evaluation

Main Achievements

- The 1st workshop of the action organized on May 30-31 (45 attendees)
- 4 STSMs planned for the next months
- 5 web-based WG meetings for a preliminary presentation of each member

Gender Balance and Early Stage Researchers

- Objectives: This COST Action will respect an appropriate gender balance and will be committed to considerably involve early stage researchers in all its activities
- Status:
  - Overall Gender Balance: 16% (in leading positions: 29%)
  - Overall Early Stage Researchers: 35% (in leading positions: 43%)
- Foreseen Support Measures: Gender balance and early stage researchers involvement will place this as a standard item on all its MC agendas. Early stage researchers will be invited to participate in MC meetings.

Dissemination

- A special session on “EU Project Information” at ETS2013
- A special session on “Counterfeit IC Identification” at VTS13
- Special issue on “Information Security Journal: A Global Perspective”

Contact details

Chair of the Action
DI NATALE Giorgio
giorgio.dinatale@lirmm.fr

Domain Committee Rapporteur
Professor JUHAR Jozef
jozef.juhar@tuke.sk

Science Officer (COST Office)
Ralph Stübner
Ralph.Stuebner@cost.eu

Website
www.trudevice.com

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