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DESIGN AND PRACTICAL IMPLEMENTATION OF A VARIABLE DUTY CYCLE CONTROL CIRCUIT FOR BRIDGE POWER CONVERTERS

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Abstract-- **Design and practical implementation of a control circuit for driving bridge converters' switches is presented in this paper. The power converter is loaded with series resonant tank and is used for induction heating of metals. By varying the output voltage duty cycle we achieve output power regulation. Digital integrated circuits are used for the design.**

Index terms-- **power converter, IGBT, duty cycle, control circuit**

1. INTRODUCTION

The presented design of the control circuit is used for driving the switches in a full-bridge power converter consisted of IGBTs and loaded with series resonant tank. This type of a power converter is commonly used for induction heating/melting of metals. Depending on the desired mode of operation, different type of gating signals may be required. Since IGBTs are voltage controlled switches, the control/driver circuit should generate voltage pulses with certain width.

The simplest type of gating signals is when the pulse width is equal to the half of the switching period. This type of a control circuit is presented in [1] and then the converter operates with constant and full power. It is appropriate for metal melting or thermal treatment of one or few types of metals. It is also more suitable for handlers who are more experienced with thermal treatment of metals.

In some applications the converter needs to operate with different output power in different cases. Power regulation can be achieved via regulating the output voltage or via regulating the switching frequency, [2]. The converter should operate on the resonant frequency in order to sustain zero voltage/current switching [3], and then the output power can only be regulated by varying the output voltage RMS value.

The output voltage RMS can be varied by varying the converter's DC supply voltage or by varying the output voltage duty cycle, [4]. For obtaining variable output duty cycle additional electronic circuit is required. This type of power regulation has the disadvantage of generating more harmonics in the output voltage associated with more RF interferences and additional component are required for eliminating them, which also increases the converter's production expenses.

In this paper a design and a practical implementation of variable duty cycle control circuit is presented. It is designed using a timing circuit, digital integrated circuits and output buffers. The same circuit can be used in a half-bridge and in a full-bridge converter topology. Also, a concept for further research plan based on microcontrollers is represented. The new control circuit would improve the performance of the present variable duty cycle control circuit.

2. THE VARIABLE DUTY CYCLE CONTROL CIRCUIT

The block diagram of the power converter with the control circuit is given on Fig. 1. The control circuit according to the reference frequency generates and sends the control signals to the driver circuit. Then the driver circuit buffers the control signals and controls the IGBTs state (on or off). The resonant load is connected at points 1 and 2 in the full-bridge converter topology.

In applications where the converter is needed to operate with variable output voltage RMS value, i.e. variable output power, the control circuit should

generate pulses with adjustable width according to the desired output power, [3], [4].

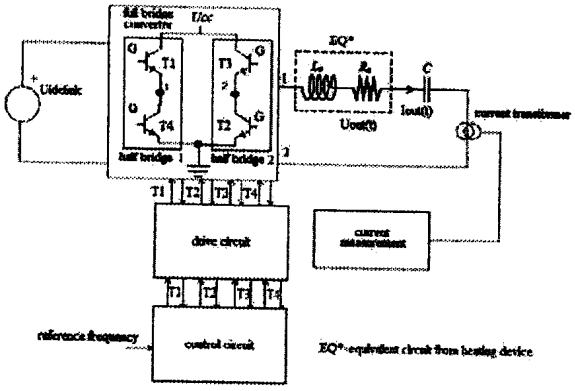


Fig. 1 – Block diagram of the power converter with the control circuit

The output voltage RMS value is defined with the following equation:

$$U_{outrms} = \sqrt{\frac{1}{T}\int_0^T u_{out}^2\ (t)dt} \tag{1}$$

Here, the duty cycle D is defined as the ratio between the pulse width and the half switching period. Then, output voltage RMS value for the first harmonic when the output voltage is square waved according to [5] is given with the equation:

$$U_2 = \frac{4V_s}{\sqrt{2}\pi}\sin\left(D\frac{\pi}{2}\right) \tag{2}$$

In (2) V_S is the DC link voltage (the same notation for the DC link voltage will be used further in the paper).

We will focus on (1) and we will derive an equation for the output voltage suitable for use with digital electronic circuit. Since digital circuits operate with binary signals, it would be appropriate if the number of digital bits n is present in the equation for the output voltage. Output voltage waveform example for duty cycle less then 1 is given on Fig. 2.

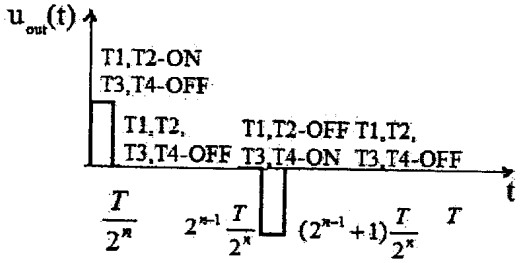


Fig. 2 – Output voltage waveform example with duty cycle less then 1

The control circuit generates square waved signals with adjustable duty cycle that drive the IGBTs in order to establish output power regulation. The person who operates with the converter will choose the appropriate duty cycle to obtain the desired output power.

If the control circuit processes signals with n bits, the switching period will be divided in time intervals with duration equal to $T/2^n$. In such case, the output voltage will be synthesized with k of these intervals, where k is a natural number and can have values from 1 to 2^{n-1}. The example on Fig. 2 is for k=1 and applying (1) in general case for n bits and k intervals with duration $T/2^n$ we obtain:

$$U_3 = \sqrt{\frac{1}{T}\left(\int_0^{k\frac{T}{2^n}} V_s^2 dt + \int_{\frac{T}{2}}^{\frac{T}{2}+k\frac{T}{2^n}} V_s^2 dt\right)} = \tag{3}$$

$$= \sqrt{\frac{2V_S^2}{T}\frac{kT}{2^n}} = V_S\sqrt{\frac{k}{2^{n-1}}}$$

This equation is appropriate for digital control of the converter. In our design we choose n=4 for the number of bits. The output voltage RMS calculations with (3) will be compared with the results obtained with simulations in the PowerSim software and with (2). The comparison is given in Table 1. The values are for a full-bridge converter topology with V_S=12 V.

Table 1. Output voltage RMS values calculated with equations and obtained with simulation

Output pulse duration	**T/16**	**2T/16**	**3T/16**	**4T/16**
U_2 [V]	2.1	4.1	6	7.6
U_3 [V]	4.2	6	7.3	8.5
Output voltage Simulated [V]	5	6.4	7.6	8.9
Output pulse duration	**5T/16**	**6T/16**	**7T/16**	**8T/16**
U_2 [V]	9	10	10.6	10.8
U_3 [V]	9.5	10.4	11.2	12
Output voltage Simulated [V]	10.1	11	11.8	12

From Table 1 we can see that the output voltage RMS values for a full-bridge converter calculated with (3) and obtained with simulation are close, and the values calculated with (2) differ for lower duty cycle values (this is due to the fact that for lower duty cycles higher harmonics dominate in the RMS value). The important part of this analysis is that the Equation (3) can be used as a basis for a digital control circuit that can regulate the output voltage RMS value, i.e. regulate the converter output power.

3. DESIGN AND PRACTICAL IMPLEMENTATION

The previously given analysis will be considered for the variable duty cycle control circuit design. According to the requirements, the control circuit should generate output voltage pulses with variable duration, from T/16 to T/2 (for n=4 we have increments of T/16). We will need two complementary outputs with equal pulse duration which will be shifted for T/2. The first output will drive IGBTs T1 and T2 in figure 1, and the second output will drive IGBTs T3 and T4. An example of these two output signals is shown in Fig. 3.

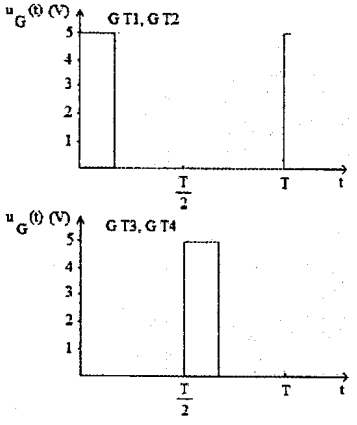


Fig.3 – Output signals that should be generated by the control circuit

The control circuit consists of an oscillator with binary counters, binary coder, pulse generator and output buffers.

The block diagram of such circuit is given in Fig. 4.

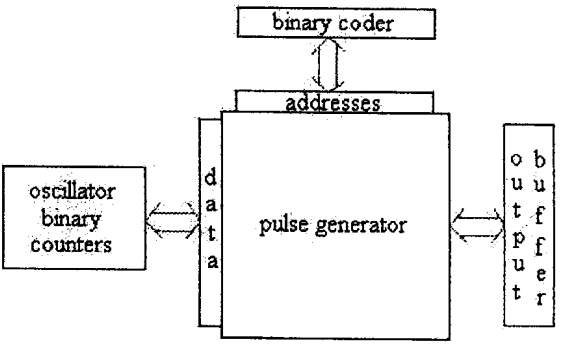


Fig. 4 – The control circuit block diagram

After the above presented analysis the control circuit is designed and practically implemented. The complete schematic diagram is given in Fig. 5 below.

The oscillator is designed with the timer integrated circuit NE555. Its frequency (point A) can be adjusted via the potentiometer P. There are two divider circuits connected at the oscillator output, IC2 and IC3 (divide by 2 and divide by 16), so the output (switching) frequency will be 32 times lower then the oscillator frequency. The switching frequency is present on Q3 output of IC3. The IC2 is used only for equalizing the pulse width from the oscillator to the half period, required when the circuit is used for driving transistors with constant and full duty cycle (D=1).

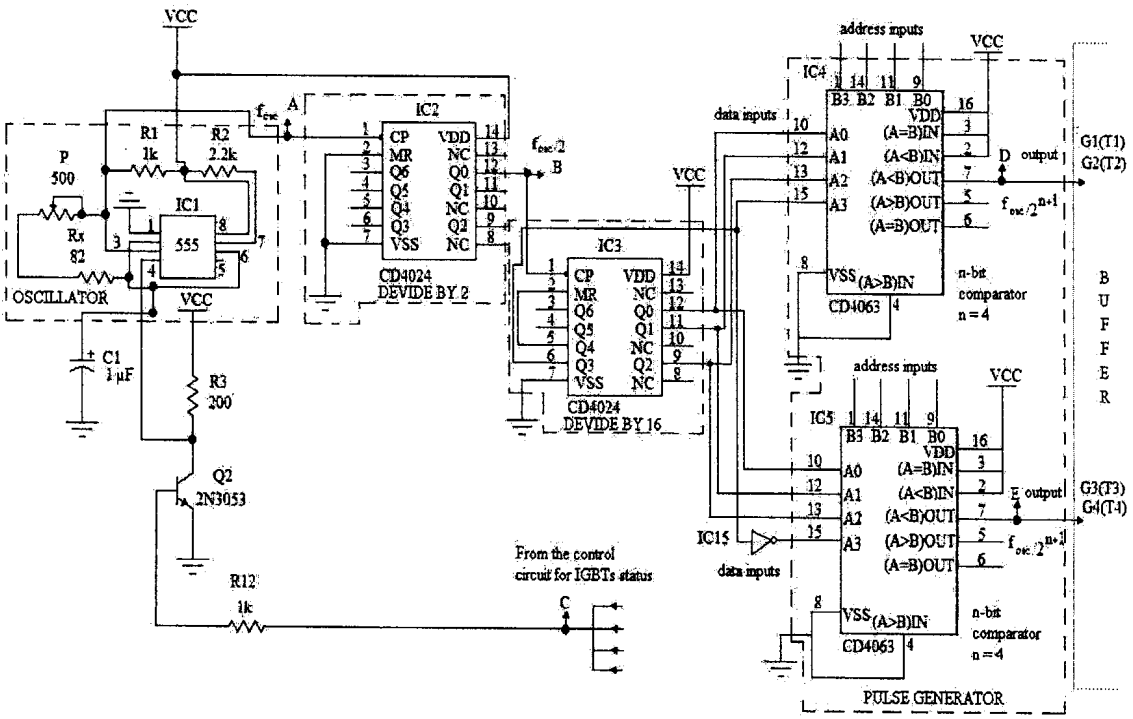


Fig. 5 – The designed control circuit schematic diagram

The main part of the control circuit is the pulse generator (Fig. 4). It has address and data inputs. The address inputs are in the binary format. Its binary combination determines the output pulses width. Data inputs are obtained from IC3's outputs Q0, Q1, Q2 and Q3. These signals are brought to the *n* bit binary comparators in the pulse generator, IC4 and IC5. These comparators have multiple outputs and for our design the output A<B is chosen. This means that while the binary combination on A input has lower or equal value (A=B input is connected to V_{CC}) then the binary combination on B input, this output will be on a high voltage level and vice versa.

The first output, point D, will be at high voltage level until the data input combination has lower value then the address input value. This output signal is used for driving IGBTs T1 and T2. The second output, point E, will be at high voltage after a half switching period. This is a requirement for the design and is achieved by inserting the inverter circuit IC15. Actually, the Q3 output on IC3 has the same frequency as the switching frequency so inverting it on A3 input of IC5 we obtain a time shift of T/2 for the second output at point E. Since, the rest of the data inputs are the same as for IC4 the pulse duration at point E will be the same as the duration at point D. The second output is used for driving IGBTs T3 and T4.

For example, if the address inputs binary combination is 0101 (binary for decimal 5), the output at point D will be on a high voltage level for data inputs combinations from 0000 to 0101 and on a low level for the rest. The output at point E will be on a high voltage level for data inputs combinations from 1000 to 1101 and on a low level for the combinations 1110 and 1111, and from 0000 to 0111. This address combination makes the output pulse duration equal to 6T/16.

In Fig. 5 point C is an input signal to the variable duty cycle control circuit. It is connected to the control circuits of the IGBT drivers and goes on high level in case of a malfunction. When this point is on a high voltage level Q2 saturates which makes low voltage level on pin 4 of the 555 IC and stops the oscillator which means the power converter stops its operation.

The binary combination for comparators address inputs can be selected via BCD switches (since the value of the half period is adjusted from T/16 to 8T/16 with T/16 increments), A/D converter or some pulse counting circuit. In our case BCD rotating switches were used.

After the presented analysis and design of the variable duty cycle control circuit, a practical implementation (prototype) is made accordingly. The practically implemented control circuit is given in Fig. 6.

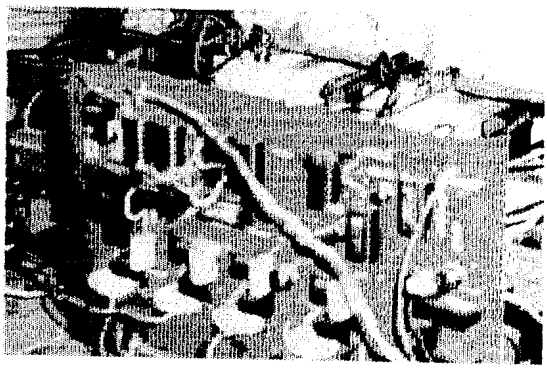
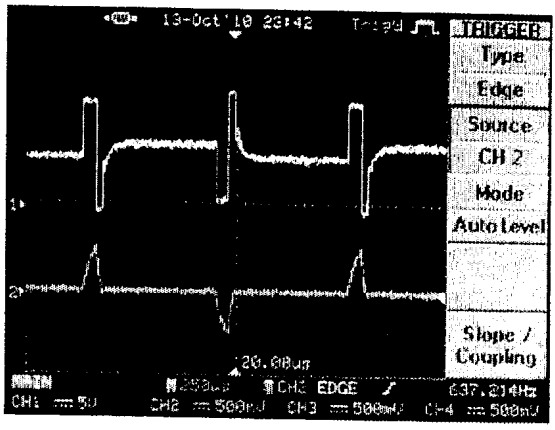
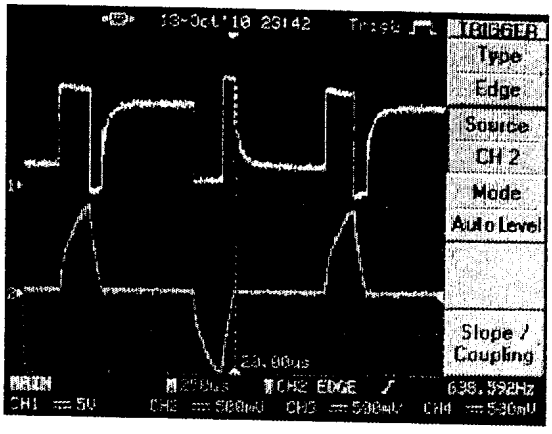


Fig. 6 – The prototype of the variable duty cycle control circuit board

The prototype control circuit was tested with full-bridge converter loaded with series resonant tank. The parameters of the resonant load are R=0.5 Ω, L=540 μH and C=55 μF, and the DC link voltage is V_S=12 V. The experimental results for pulse duration T/16 and 3T/16 are given in Fig. 7, a) and b), respectively. The upper waveforms are for the output voltage and the one below is for the output current.



a)



b)

Fig. 7 – Output voltage and current waveforms for the full-bridge power converter loaded with series resonant tank and variable duty cycle

The experimental results for all pulse durations are presented in Table 2. The oscillator frequency (point A on Fig. 5) during testing was f_{OSC}=20.4 kHz, which gives output frequency (points D and E on Fig. 5) of 638 Hz.

Table 2. Experimental results

Pulse duration	**T/16**	**2T/16**	**3T/16**	**4T/16**
IGBTs T1,T2 ON T3,T4 angles [°]	0-23 180-203	0-45 180-225	0-68 180-248	0-90 180-270
k	1	2	3	4
V_{OUT} [V] resistive load	4.24	6	7	8.5
V_{out} [V] RLC load	5.2	7	7.8	9
I_{OUT} [A] RLC load	0.13	0.58	1.32	1.72
Pulse duration	**5T/16**	**6T/16**	**7T/16**	**8T/16**
IGBTs T1,T2 ON T3,T4 angles [°]	0-123 180-293	0-145 180-315	0-168 180-338	0-180 180-360
k	5	6	7	8
V_{OUT} [V] resistive load	9.5	10.3	11.2	12
V_{out} [V] RLC load	10.2	10.9	11.8	12
I_{OUT} [A] RLC load	2.28	2.95	3.5	4.1

The measured output voltage for resistive load in Table 3 has values according to the calculated in Table 2. For RLC load the output voltage differs because the free-wheeling diodes of the transistors are conducting in part of the switching period (this can be seen on Fig. 7).

4. FUTURE RESEARCH PLAN

According to the requirements, a concept using a microcontroller unit (MCU) is suggested. Using microcontrollers, the design of the variable duty cycle control circuit can be simplified, [6], [7]. Nowadays, there are many manufacturers that produce low cost microcontrollers. The new control circuit would have only a few external components. All of the blocks in Fig. 5, except the output buffer, would be integrated in the microcontroller and the functions will be defined with the program code written in its program memory. The output and input signals can be connected directly to the microcontroller input/output pins. The only complexity is that the program code must be build or compiled, and further written in the program memory of the microcontroller. This can be done in assembler, C or some other programming language and is relatively simple (depending on the requirements) when using 8-bit microcontrollers. The block-diagram of the suggested microcontroller unit is given in Fig. 8.

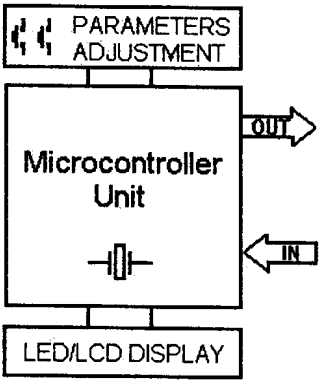


Fig. 8 – Microcontroller unit block-diagram

As shown on Fig. 8 directly connected displays can be used for parameters monitoring or reading the adjusted parameters. Adjusting is accomplished by pressing the buttons connected to the MCU and their function is defined in the MCU program memory.

Microcontrollers have many input/output pins (depending on the model, from several to few tens of input/output pins), hence many of them can be used for additional inputs if necessary (from protection circuits or other) to achieve additional operation controls or state indications.

Some of the improvements of the suggested MCU control circuit are:

- ✓ Greater reliability;
- ✓ Simplified electronic circuit;
- ✓ More features can be implemented easily on the same circuit board;
- ✓ Greater duty cycle resolution can be achieved;
- ✓ Improved parameters monitoring and adjustment.

5. CONCLUSION

The design of the presented control circuit can be used for gating full-bridge or half-bridge series resonant converters in cases when output power needs regulation.

The main part of the control circuit is the pulse generator (Fig. 4). It has address and data inputs. The address inputs are in the binary format. Its binary combination determines the output pulses width. Data inputs are obtained from IC3's outputs Q0, Q1, Q2 and Q3. These signals are brought to the *n* bit binary comparators in the pulse generator, IC4 and IC5. These comparators have multiple outputs and for our design the output A<B is chosen. This means that while the binary combination on A input has lower or equal value (A=B input is connected to V_{CC}) then the binary combination on B input, this output will be on a high voltage level and vice versa.

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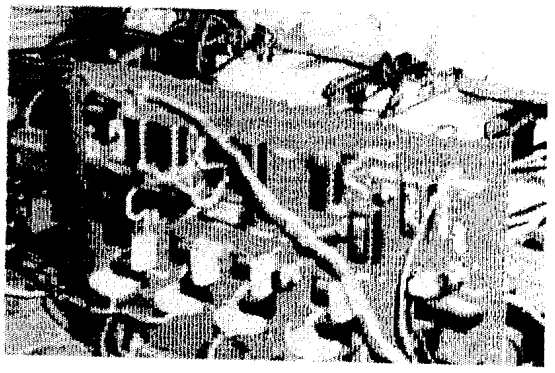

Fig. 6 – The prototype of the variable duty cycle control circuit board

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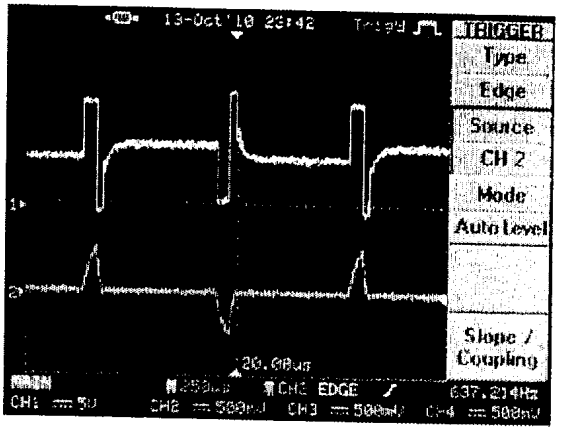
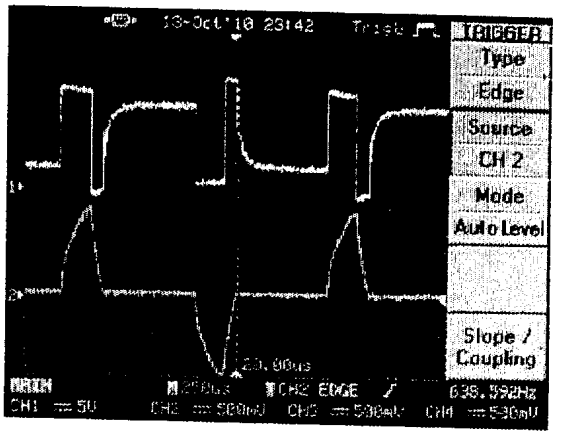


a)



b)

Fig. 7 – Output voltage and current waveforms for the full-bridge power converter loaded with series resonant tank and variable duty cycle

The practically implemented circuit according to the design presented in the paper gives acceptable results for use in series resonant power converters for induction heating with regulating the output power via changing the output voltage duty cycle.

Future upgrade can be implemented according to the presented concept that includes microcontroller unit which incorporates all of the blocks in the previously designed control circuit.

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